VLSI and hardware engineering interview questions

- Explain why & how a MOSFET works

- Draw Vds-Ids curve for a MOSFET. Now, show how this curve changes (a) with increasing Vgs (b) with increasing transistor width (c) considering Channel Length Modulation

- Explain the various MOSFET Capacitances & their significance

- Draw a CMOS Inverter. Explain its transfer characteristics

- Explain sizing of the inverter

- How do you size NMOS and PMOS transistors to increase the threshold voltage?

- What is Noise Margin? Explain the procedure to determine Noise Margin

- Give the expression for CMOS switching power dissipation

- What is Body Effect?

- Describe the various effects of scaling

- Give the expression for calculating Delay in CMOS circuit

- What happens to delay if you increase load capacitance?

- What happens to delay if we include a resistance at the output of a CMOS circuit?

- What are the limitations in increasing the power supply to reduce delay?

- How does Resistance of the metal lines vary with increasing thickness and increasing length?

- You have three adjacent parallel metal lines. Two out of phase signals pass through the outer two metal lines. Draw the waveforms in the center metal line due to interference. Now, draw the signals if the signals in outer metal lines are in phase with each other

- What happens if we increase the number of contacts or via from one metal layer to the next?

- Draw a transistor level two input NAND gate. Explain its sizing (a) considering Vth (b) for equal rise and fall times

- Let A & B be two inputs of the NAND gate. Say signal A arrives at the NAND gate later than signal B. To optimize delay, of the two series NMOS inputs A & B, which one would you place near the output?

- Draw the stick diagram of a NOR gate. Optimize it

- For CMOS logic, give the various techniques you know to minimize power consumption

- What is Charge Sharing? Explain the Charge Sharing problem while sampling data from a Bus

- Why do we gradually increase the size of inverters in buffer design? Why not give the output of a circuit to one large inverter?

- In the design of a large inverter, why do we prefer to connect small transistors in parallel (thus increasing effective width) rather than lay out one transistor with large width?

- Given a layout, draw its transistor level circuit. (I was given a 3 input AND gate and a 2 input Multiplexer. You can expect any simple 2 or 3 input gates)

- Give the logic expression for an AOI gate. Draw its transistor level equivalent. Draw its stick diagram

- Why don't we use just one NMOS or PMOS transistor as a transmission gate?

- For a NMOS transistor acting as a pass transistor, say the gate is connected to VDD, give the output for a square pulse input going from 0 to VDD

- Draw a 6-T SRAM Cell and explain the Read and Write operations

- Draw the Differential Sense Amplifier and explain its working. Any idea how to size this circuit? (Consider Channel Length Modulation)

- What happens if we use an Inverter instead of the Differential Sense Amplifier?

- Draw the SRAM Write Circuitry

- Approximately, what were the sizes of your transistors in the SRAM cell? How did you arrive at those sizes?

- How does the size of PMOS Pull Up transistors (for bit & bit- lines) affect SRAM's performance?

- What's the critical path in a SRAM?

- Draw the timing diagram for a SRAM Read. What happens if we delay the enabling of Clock signal?

- Give a big picture of the entire SRAM Layout showing your placements of SRAM Cells, Row Decoders, Column Decoders, Read Circuit, Write Circuit and Buffers

- In a SRAM layout, which metal layers would you prefer for Word Lines and Bit Lines? Why?

- How can you model a SRAM at RTL Level?

- What's the difference between Testing & Verification?

- For an AND-OR implementation of a two input Mux, how do you test for Stuck-At-0 and Stuck-At-1 faults at the internal nodes? (You can expect a circuit with some redundant logic)

- What is Latch Up? Explain Latch Up with cross section of a CMOS Inverter. How do you avoid Latch Up?

Verilog Center Sample Questions asked in Interviews

Rajesh Bawankule

Introduction :

A fresh graduate faces some tough questions in his first job interview. The questions themselves are simple but require practical and innovative approach to solve them. I started collecting some questions from my own experience and from my friends. Answers to most questions are not given. Spend some time to solve these and let me know if you have some more interesting ones.

Please do not send me emails asking for solutions. You are not supposed to answer these questions in 10 seconds like some university multiple choice questions. Some questions may have more than correct answers and some may not even have correct answer :)

What matters is your approach to solution and understanding of basic hardware design principles.

Recently added questions

Q. Design a logic which mimics a infinite width register. It takes input serially 1 bit at a time. Output is asserted high when this register holds a value which is divisible by 5.

For example:

Input	Sequence	Value	Output
1	1	1	0
0	10	2	0
1	101	5	1
0	1010	10	1
1	10101	21	0

(Hint: Use a FSM to create this)

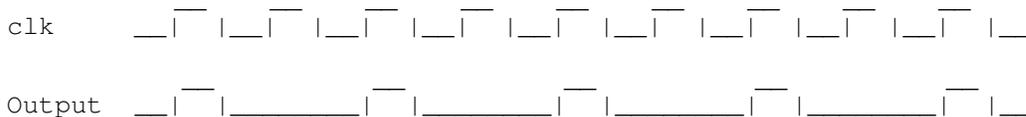Q.Design a block which has 3 inputs as followed.
   1. system clock of pretty high freq
   2. asynch clock input P
   3. asynch clock input Q

        P and Q clocks have 50% duty cycle each. Their frequencies are close enough
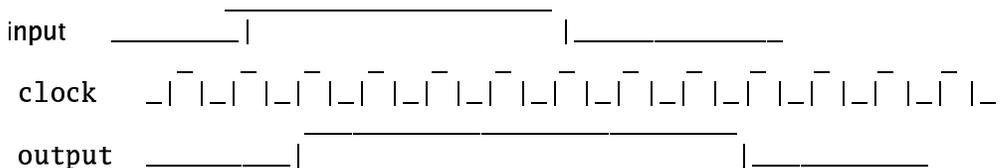   and they have phase difference. Design the block to generate these outputs.

   1. PeqQ : goes high if periods of P and Q are same
   2. PleQ : goes high if P's period is less than that of Q.
   3. PgrQ : goes high if P's period is greater than that of Q.

Q. What's the difference between a latch and a flip-flop? Write Verilog RTL code for each. (This is one of the most common questions but still some EE's don't know how to explain it correctly!)

Q. Design a black box whose input clock and output relationship as shown in diagram.

```
           __    __    __    __    __    __    __    __    __
clk     __|  |__|  |__|  |__|  |__|  |__|  |__|  |__|  |__|  |__

           __                __                __                __
Output  __|  |_____|  |_____|  |_____|  |_____|  |__
```


Q. Design a digital circuit to delay the negative edge of the input
   signal by 2 clock cycles.

```
            _____
 input  _____|                            |_____

          _  _  _  _  _  _  _  _  _  _  _  _  _  _  _  _
 clock   _| |_| |_| |_| |_| |_| |_| |_| |_| |_| |_| |_| |_| |_| |_| |_

                        _____
 output  _____|                                    |_____
```

Q. Design a Pattern matching block

- Output is asserted if pattern "101" is detected in last 4 inputs.
- How will you modify this design if it is required to detect same "101" pattern anywhere in last 8 samples?

Questions:

Q1.

The digital circuit is shown with logic delay (dly3) and two clock buffer delays (dly1, dly2).

- How will you fix setup timing violations occurring at pin B?
- How will you fix hold violations occurring at pin B?

(Hint: Change the values of three delays to get desired effect)

Q2.

Sender sends data at the rate of 80 words / 100 clocks
Receiver can consume at the rate of 8 words / 10 clocks

Calculate the depth of FIFO so that no data is dropped.
Assumptions: There is no feedback or handshake mechanism. Occurrence of data in that time period is guaranteed but exact place in those clock cycles is indeterminate.

Q3

Optical sensors A and B are positioned at 90 degrees to each other as shown in Figure. Half od the disc is white and remaining is black. When black portion is under sensor it generates logic 0 and logic 1 when white portion is under sensor.

Design Direction finder block using digital components (flip flops and gates) to indicate speed. Logic 0 for clockwise and Logic 1 for counter clockwise.

Q4

Will this design work satisfactorily?
Assumptions: thold = tsetup = tclock_out = tclock_skew = 1ns.
After reset A = 0, B = 1

1. Design a 4:1 mux in Verilog.
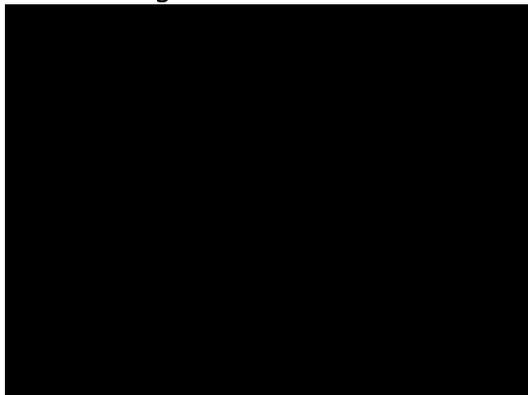
- Multiple styles of coding. e.g.
  Using **if-else** statements

```
if(sel_1 == 0 && sel_0 == 0) output = I0;
else if(sel_1 == 0 && sel_0 == 1) output = I1;
else if(sel_1 == 1 && sel_0 == 0) output = I2;
else if(sel_1 == 1 && sel_0 == 1) output = I3;
```

Using **case** statement

```
case ({sel_1, sel_0})
    00 : output = I0;
    01 : output = I1;
    10 : output = I2;
    11 : output = I3;
    default : output = I0;
endcase
```

- What are the advantages / disadvantages of each coding style shown above?

- How Synthesis tool will give result for above codes?

- What happens if default statement is removed in case statement?

- What happens if combination 11 and default statement is removed? (Hint Latch inference)
  (Comments : Though this questions looks simple and out of text books, the answers to supporting questions can come only after some experience / experimentation

Design a FSM (Finite State Machine) to detect a sequence 10110.
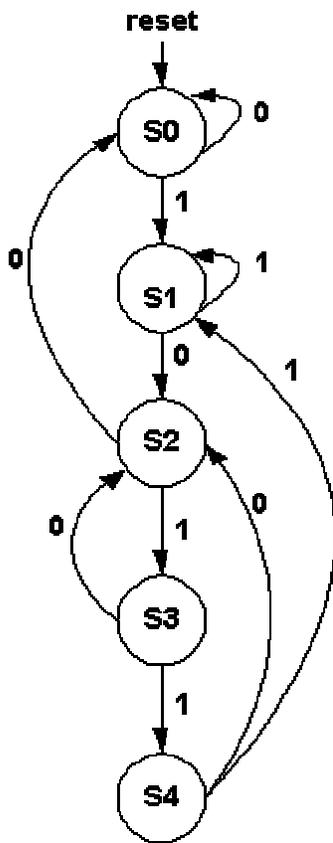
**State Transition Diagram**
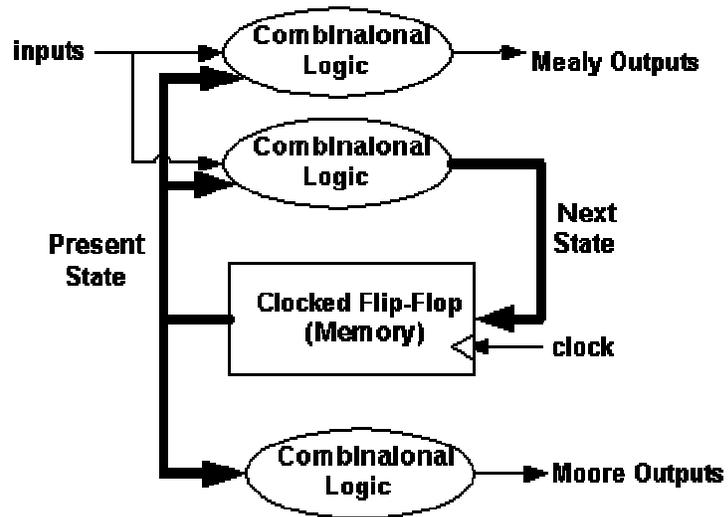
FSM Block Diagram

- Have a good approach to solve the design problem.

- Know the difference between Mealy, Moore, 1-Hot type of state encoding.

- Each state should have output transitions for all combinations of inputs.

- All states make transition to appropriate states and not to default if sequence is broken.
  e.g. S3 makes transition to S2 in example shown.

- Take help of FSM block diagram to write Verilog code.

3. One more sequence detector:

Design a FSM (Finite State Machine) to detect more than one "1"s in last 3 samples.
For example: If the input sampled at clock edges is 0 1 0 1 0 1 1 0 0 1
then output should be 0 0 0 1 0 1 1 1 0 0 as shown in timing diagram.

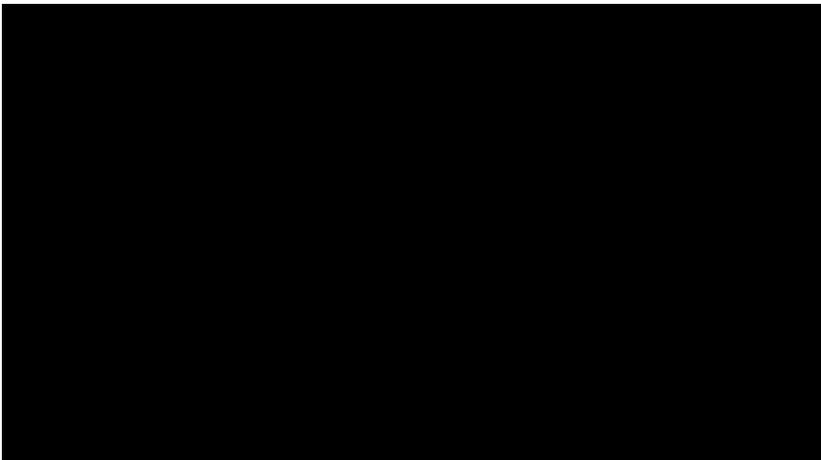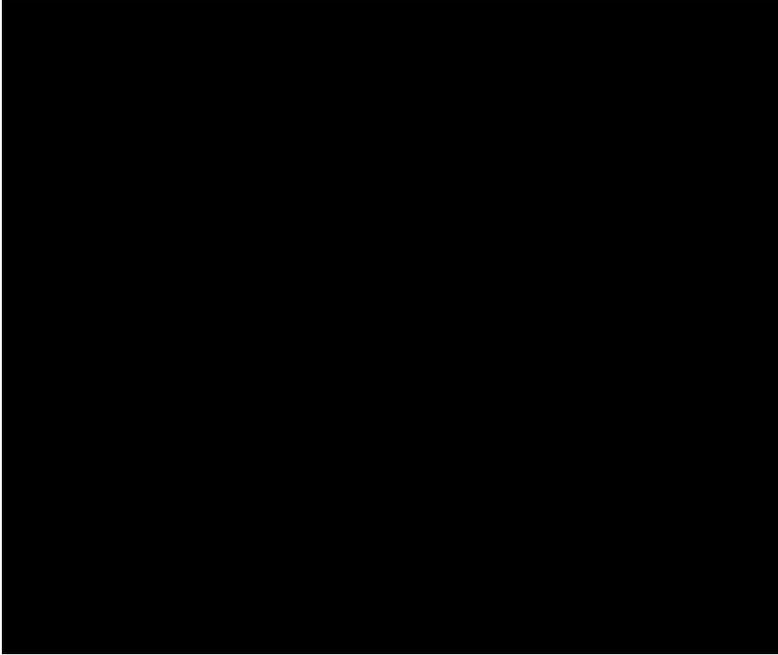And yes, you have to design this FSM using not more than 4 states!!
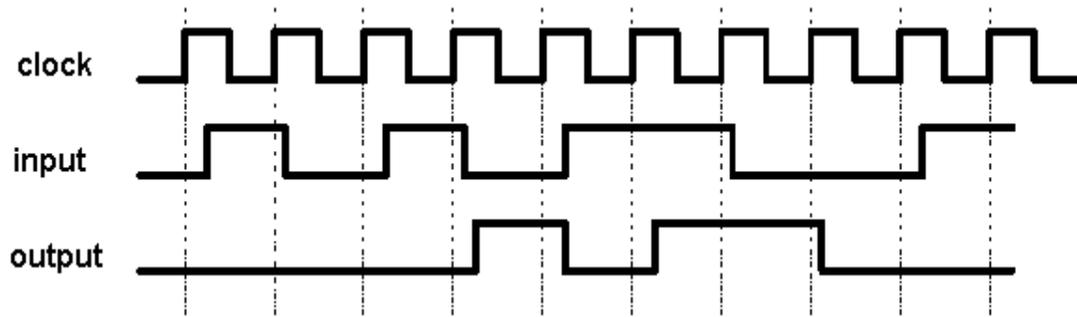
4. Design a state machine to divide the clock by 3/2.
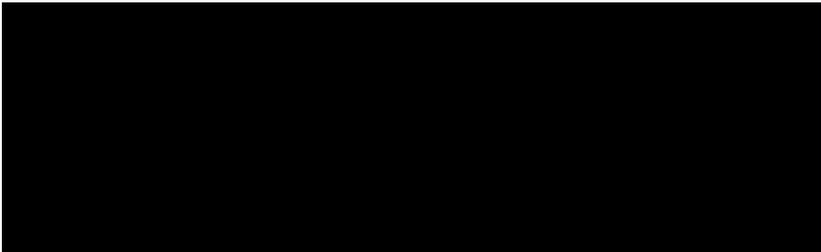
(Hint: 2 FSMs working on posedge and negedge)

5. Draw timing diagrams for following circuit.

- What is the maximum frequency at which this circuit can operate?

- What is the minimum width of input pulse and position?

- Problem can be given interesting twist by specifying all delays in min and max types.

6. Design a Digital Peak Detector in Verilog.

7. Design a RZ (return to zero)circuit. Design a clock to pulse circuit in Verilog / hardware gates.
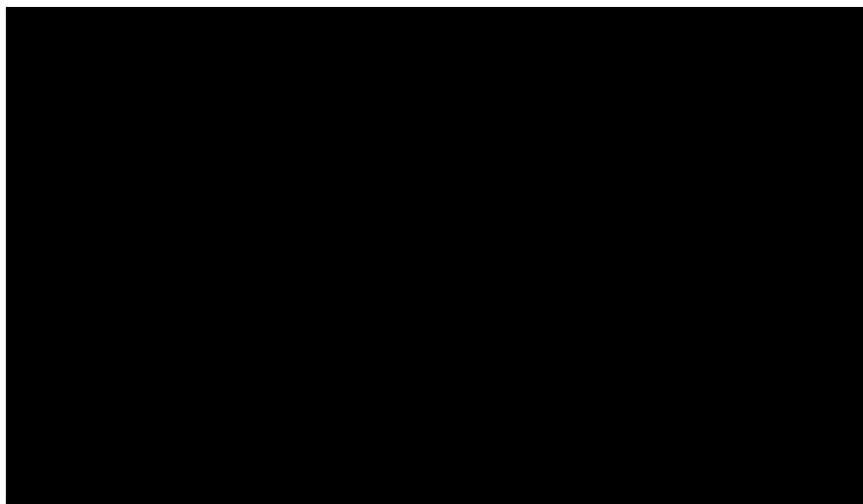
8. Miscellaneous Basic Verilog Questions:

- What is the difference between Behavior modeling and RTL modeling?

- What is the benefit of using Behavior modeling style over RTL modeling?

- What is the difference between blocking assignments and non-blocking assignments ?

- How do you implement the bi-directional ports in Verilog HDL

- How to model inertial and transport delay using Verilog?

- How to synchronize control signals and data between two different clock domains?

VLSI Design:

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30) Draw the Differential Sense Amplifier and explain its working. Any idea how to size this circuit? (Consider Channel Length Modulation)

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33) Approximately, what were the sizes of your transistors in the SRAM cell? How did you arrive at those sizes?

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41) For an AND-OR implementation of a two input Mux, how do you test for Stuck-At-0 and Stuck-At-1 faults at the internal nodes? (You can expect a circuit with some redundant logic)

42) What is Latch Up? Explain Latch Up with cross section of a CMOS Inverter. How do you avoid Latch Up?

Digital Design:

1) Give two ways of converting a two input NAND gate to an inverter

2) Given a circuit, draw its exact timing response. (I was given a Pseudo Random Signal Generator; you can expect any sequential ckt)

3) What are set up time & hold time constraints? What do they signify? Which one is critical for estimating maximum clock frequency of a circuit?

4) Give a circuit to divide frequency of clock cycle by two

5) Design a divide-by-3 sequential circuit with 50% duty circle. (Hint: Double the Clock)

6) Suppose you have a combinational circuit between two registers driven by a clock.
What will you do if the delay of the combinational circuit is greater than your
*

A:### BEGIN PERL SNIPET ###

```perl
        for ($i = 1; $i <= (($input * 2) - 1); $i += 2) {

            if ($i <= $input) {

                $stars = $i;

                $spaces = ($input - $stars) / 2;

                while ($spaces--) { print " "; }

                while ($stars--) { print "*"; }

            } else {

                $spaces = ($i - $input) / 2;

                $stars = $input - ($spaces * 2);

                while ($spaces--) { print " "; }

                while ($stars--) { print "*"; }

            }

            print "\n";

        }

        ### END PERL SNIPET ###
```
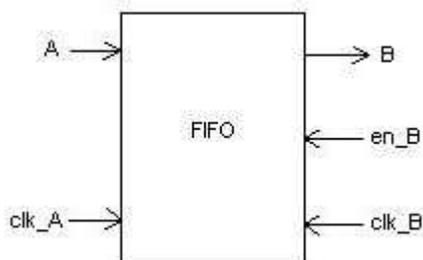
General Answer 1

Q: Given the following FIFO and rules, how deep does the FIFO need to be to
    prevent underflowing or overflowing?

RULES:

1) frequency(clk_A) = frequency(clk_B) / 4
2) period(en_B) = period(clk_A) * 100
3) duty_cycle(en_B) = 25%

A:

Assume clk_B = 100MHz (10ns)

From (1), clk_A = 25MHz (40ns)

From (2), period(en_B) = 40ns * 400 = 4000ns, but we only
output for 1000ns,   due to (3), so 3000ns of the enable we
are doing no output work.Therefore, FIFO size = 3000ns/40ns
= 75 entries.

General Answer 2

Q: Draw the state diagram to output a "1" for one cycle
   if the sequence "0110" shows up (the leading 0s cannot be
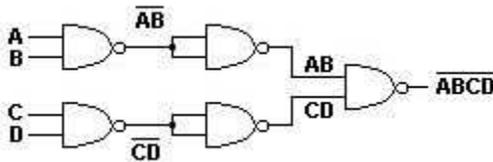   used in more than one sequence).

A:
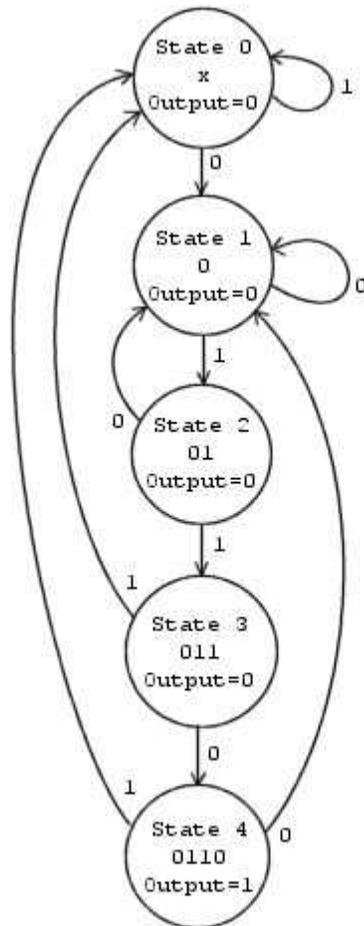
Q: Design a four-input NAND gate using only two-input NAND gates.

A: Basically, you can tie the inputs of a NAND gate together to get an inverter, so...

Q: Draw the state diagram for a circuit that outputs a "1" if the aggregate serial
   binary input is divisible by 5. For instance, if the input stream is 1, 0, 1, we
   output a "1" (since 101 is 5). If we then get a "0", the aggregate total is 10, so
   we output another "1" (and so on).

A: We don't need to keep track of the entire string of numbers - if something

   is divisible by 5, it doesn't matter if it's 250 or 0, so
   we can just reset to 0.

   So we really only need to keep track of "0" through "4".
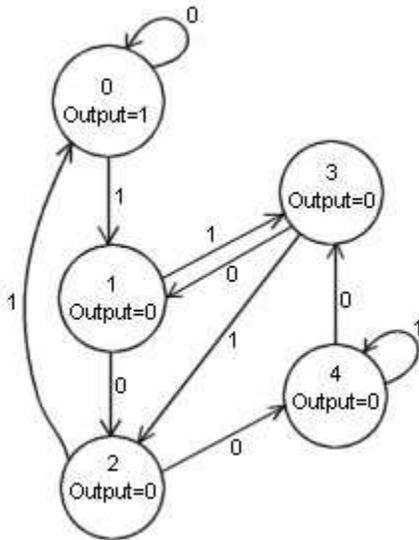
7) The answer to the above question is breaking the combinational circuit and pipelining it. What will be affected if you do this?

8) What are the different Adder circuits you studied?

9) Give the truth table for a Half Adder. Give a gate level implementation of the same.

10) Draw a Transmission Gate-based D-Latch.

11) Design a Transmission Gate based XOR. Now, how do you convert it to XNOR? (Without inverting the output)

12) How do you detect if two 8-bit signals are same?

13) How do you detect a sequence of "1101" arriving serially from a signal line?

14) Design any FSM in VHDL or Verilog.

- INTEL questions

- Insights of an inverter. Explain the working?

- Insights of a 2 input NOR gate. Explain the working?

- Insights of a 2 input NAND gate. Explain the working?

- Implement F= not (AB+CD) using CMOS gates?

- Insights of a pass gate. Explain the working?

- Why do we need both PMOS and NMOS transistors to implement a pass gate?

- What does the above code synthesize to?

- Cross section of a PMOS transistor?

- Cross section of an NMOS transistor?

- What is a D-latch? Write the VHDL Code for it?

- Differences between D-Latch and D flip-flop?

- Implement D flip-flop with a couple of latches? Write a VHDL Code for a D flip-flop?

- What is latchup? Explain the methods used to prevent it?

- What is charge sharing?

- While using logic design, explain the various steps that r followed to obtain the desirable design in a well defined manner?

- Why is OOPS called OOPS? (C++)

- What is a linked list? Explain the 2 fields in a linked list?

- Implement a 2 I/P and gate using Tran gates?

- Insights of a 4bit adder/Sub Circuit?

- For f = AB+CD if B is S-a-1, what r the test vectors needed to detect the fault?

- Explain various adders and diff between them?

- Explain the working of 4-bit Up/down Counter?

- A circuit has 1 input X and 2 outputs A and B. If X = HIGH for 4 clock ticks, A = 1. If X = LOW for 4 clock ticks, B = 1. Draw a state diagram for this Spec?

- Advantages and disadvantages of Mealy and Moore?

- Id vs. Vds Characteristics of NMOS and PMOS transistors?

- Explain the operation of a 6T-SRAM cell?

- Differences between DRAM and SRAM?

- Implement a function with both ratioed and domino logic and merits and demerits of each logic?

- Given a circuit and asked to tell the output voltages of that circuit?

- How can you construct both PMOS and NMOS on a single substrate?

- What happens when the gate oxide is very thin?

- What is setup time and hold time?

- Write a pseudo code for sorting the numbers in an array?

- What is pipelining and how can we increase throughput using pipelining?

- Explain about stuck at fault models, scan design, BIST and IDDQ testing?

- What is SPICE?

- Differences between IRSIM and SPICE?

- Differences between netlist of HSPICE and Spectre?

- What is FPGA?

- Draw the Cross Section of an Inverter? Clearly show all the connections between M1 and poly, M1 and diffusion layers etc?

- Draw the Layout of an Inverter?

- If the current thru the poly is 20nA and the contact can take a max current of 10nA how would u overcome the problem?

- Implement F = AB+C using CMOS gates?

- Working of a 2-stage OPAMP?

- 6-T XOR gate?

- Differences between blocking and Non-blocking statements in Verilog?

- Differences between Signals and Variables in VHDL? If the same code is written using Signals and Variables what does it synthesize to?

- Differences between functions and Procedures in VHDL?

- What is component binding?

- What is polymorphism? (C++)

- What is hot electron effect?

- Define threshold voltage?

- Factors affecting Power Consumption on a chip?

- Explain Clock Skew?

- Why do we use a Clock tree?

- Explain the various Capacitances associated with a transistor and which one of them is the most prominent?

- Explain the Various steps in Synthesis?

- Explain ASIC Design Flow?

- Explain Custom Design Flow?

- Why is Extraction performed?

- What is LVS, DRC?

- Who provides the DRC rules?

- What is validation?

- What is Cross Talk?

- Different ways of implementing a comparator?

- What r the phenomenon which come into play when the devices are scaled to the sub-micron lengths?

- What is clock feed through?

- Implement an Inverter using a single transistor?

- What is Fowler-Nordheim Tunneling?

- Insights of a Tri-state inverter?

- If an/ap = 0.5, an/ap = 1, an/ap = 3, for 3 inverters draw the transfer characteristics?

- Differences between Array and Booth Multipliers?

- Explain the concept of a Clock Divider Circuit? Write a VHDL code for the same?

- Which gate is normally preferred while implementing circuits using CMOS logic, NAND or NOR? Why?

- Insights of a Tri-State Inverter?

- Basic Stuff related to Perl?

- Have you studied buses? What types?

- Have you studied pipelining? List the 5 stages of a 5 stage pipeline. Assuming 1 clock per stage, what is the latency of an instruction in a 5 stage machine? What is the throughput of this machine ?

- How many bit combinations are there in a byte?

- For a single computer processor computer system, what is the purpose of a processor cache and describe its operation?

- Explain the operation considering a two processor computer system with a cache for each processor.

- What are the main issues associated with multiprocessor caches and how might you solve them?

- Explain the difference between write through and write back cache.

- Are you familiar with the term MESI?

- Are you familiar with the term snooping?

- Describe a finite state machine that will detect three consecutive coin tosses (of one coin) that results in heads.

- In what cases do you need to double clock a signal before presenting it to a synchronous state machine?

- You have a driver that drives a long signal & connects to an input device. At the input device there is either overshoot, undershoot or signal threshold violations, what can be done to correct this problem?

- What are the total number of lines written by you in C/C++? What is the most complicated/valuable program written in C/C++?

- What compiler was used?

- What is the difference between = and == in C?

- Are you familiar with VHDL and/or Verilog?

- What types of CMOS memories have you designed? What were their size? Speed?

- What work have you done on full chip Clock and Power distribution? What process technology and budgets were used?

- What types of I/O have you designed? What were their size? Speed? Configuration? Voltage requirements?

- Process technology? What package was used and how did you model the package/system? What parasitic effects were considered?

- What types of high speed CMOS circuits have you designed?

- What transistor level design tools are you proficient with? What types of designs were they used on?

- What products have you designed which have entered high volume production?

- What was your role in the silicon evaluation/product ramp? What tools did you use?

- If not into production, how far did you follow the design and why did not you see it into production?

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- What work have you done on full chip Clock and Power distribution? What process technology and budgets were used?

- What types of I/O have you designed? What were their size? Speed? Configuration? Voltage requirements?

- Process technology? What package was used and how did you model the package/system? What parasitic effects were considered?

- What types of high speed CMOS circuits have you designed?

- What transistor level design tools are you proficient with? What types of designs were they used on?

- What products have you designed which have entered high volume production?

- What was your role in the silicon evaluation/product ramp? What tools did you use?

- If not into production, how far did you follow the design and why did not you see it into production?

Electrical enginr questions

- What types of CMOS memories have you designed? What were their size? Speed? Configuration Process technology?

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- Two capacitors are connected in parallel through a switch. C1= 1uF, C2= 0.25uF. Initially switch is open,C1 is charged to 10V. What happens if we close the switch?No loss in the wires and capacitors.
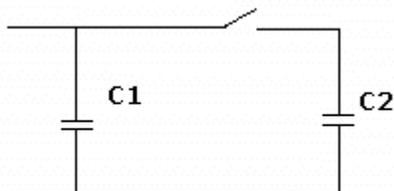
- You have 2 switches to control the light in the long corridor. You want to be able to turn the light on entering the corridor and turn it off at the other end. Do the wiring circuit.

- This question is based on the previous one, but there are 3 switches that can turn on and off a light in the room. How to wire them up?

- What will be the voltage level between the 2 capacitors? The Vcc = 10v DC.
 *Sent by Tanh, VLSI engineer*
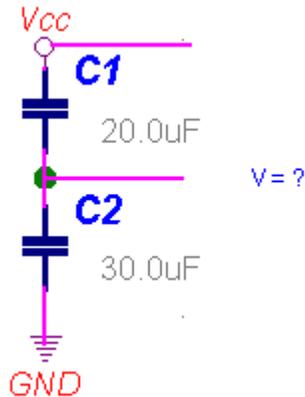
Hint from Hitequest

- Suppose, you work on a specification for a system with some digital parameters. Each parameter has Min,Typ and Max colomns. In what column would you put a Setup time and a Hold time?

- Design a simple circuit based on combinational logic to double the output frequency.
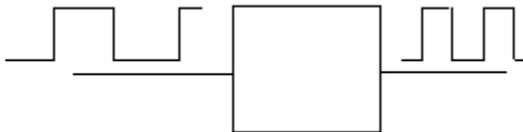
- 8bit ADC with parallel output converts input signal into digital numbers. You have to come up with the idea of a circuit , that finds MAX of every 10 numbers at the output of the ADC.

- Implement comparator that compares two 2-bit numbers A and B. The comparator should have 3 outputs: A > B, A < B, A = B. Do it two ways:
  - using combinational logic;
  - using multiplexers. Write HDL code for your schematic at RTL and gate level.

A   A>B

A=B

B   A<B
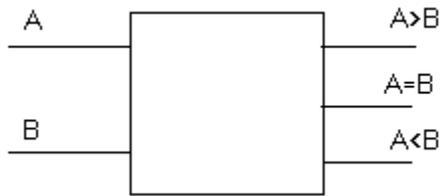
- You have 8 bit ADC clocking data out every 1mS. Design a system that will sort the output data and keep a statistics how often each binary number appears at the output of ADC.
  What types of flip-flops do you know?

- Implement D- latch from
  - RS flip flop;
  - multiplexer.

- How to convert D-latch into JK-latch and JK-latch into D-latch?

- You have two counters to 16, built from negedge D- FF . First circuit is synchronous and second is "ripple" (cascading). Which circuit has a less propagation delay?

- what is the difference between flip-flop and latch?
  Write an HDL code for their behavioral models.

  Describe the operation of DAC? What are the most important parameters of DAC? Do we really need both INL and DNL to estimate linearity?

- Compare briefly all types of ADC,that you know .

- How will the output signal of an ideal integrator look like after
  - a positive pulse is applied to the input;
  - a series of 10 positive pulses ?

- How to design a divide-by-3 counter with equal duty cycle ?
  question from Anonymous

- For an 8-bit flash A/D converter with an input range from 0V to 2.55V, describe what happens when the input voltage changes from 1.27V to 1.28V

- Your system has CPU, ALU and two 8bit registers. There is no external memory. Can you swap the contence of the registers ?

- I swapped 2 transistors in CMOS inverter (put n-transistor at the top and p-transistor at the bottom). Can this circuit work as a noninverting buffer?
 (By E.Martovetsky,design eng from Transmeta)
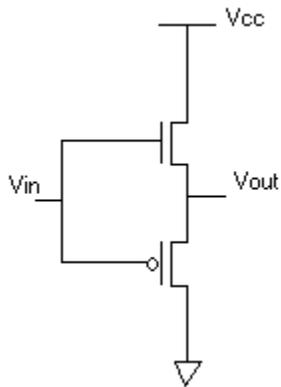
- Convert D-latch into divider by 2.
  What is the max clock frequency the circuit can handle ?
  T_setup= 6nS
  T_hold = 2nS
  T_propagation = 10nS

- The circle can rotate clockwise and back. Use minimum hardware to build a circuit to indicate the direction of rotating.
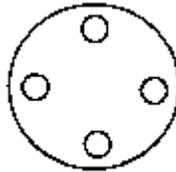

- For ATE engineers (semiconductor test):
  Draw a shmoo plot of two parameters: Clock period Tclk and setup time Tsetup.

- For chip design/test/product engineers :
  An IC device draws higher current when temperature gets:
  - higher
  - lower

Hint from Hitequest

- enter the office people have to pass through the corridor. Once someone gets into the office the light turns on. It goes off when noone is present in the room. There are two registration sensors in the corridor. Build a state machine diagram and design a circuit to control the light.

light

s1   s2
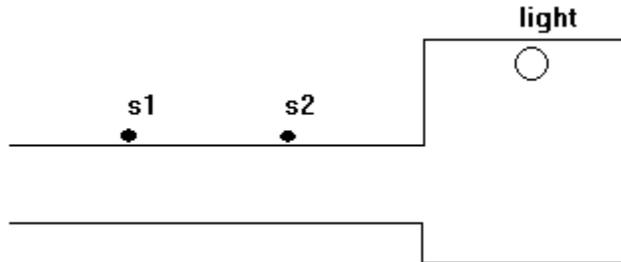
- A voltage source with internal impedance Z_source = 50 OHm is connected to a transmission line with Z = 50 OHm. Z_load is also 50 OHm.
  The voltage source generates a single voltage step 1V.
  What will be the voltage level on the load:

  a) 2V , because the reflected signal will be in-phase with the incident signal;
  b) 0.33V , because the voltage is devided between Z_source , Z_load and Z_transm.line;
  c) 0.5V , because the voltage is devided between Z_source and Z_load.
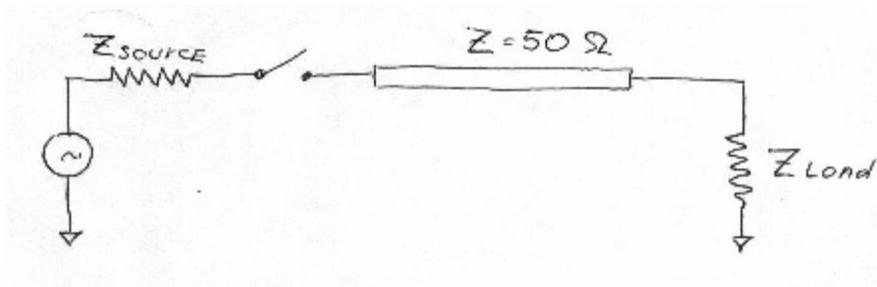
- Draw a transistor schematic of NOR gate,it's layout and a cross section of the layout.
  This question is quite popular.

- The silicon of a new device has memory leak. When all "0" are written into RAM, it reads back all "0" whithout any problem. When all "1" are written, only 80% of memory cells are read back correctly. What can be possibly the problem with the RAM?
  Michael Altshuler, product engineer.

- Draw a CMOS inverter. Why does CMOS technology dominate in VLSI manufacturing?

  Leon Backer, DFT engineer

- Design a FIFO 1 byte wide and 13 words deep. The FIFO is interfacing 2 blocks with different clocks. On the rising edge of clk the FIFO stores data and increments wptr. On the rising edge of clkb the data is put on the b-output,the rptr points to the next data to be read.
  If the FIFO is empty, the b-output data is not valid. When the FIFO is full the existing data should not be overriden.
  When rst_N is asserted, the FIFO pointers are asynchronously reset.

  module fifo1 (full,empty,clk,clkb,ain,bout,rst_N)
  output [7:0] bout;
  input [7:0] ain;
  input clk,clkb,rst_N;
  output empty, full;
  reg [3:0] wptr, rptr;
  ...

  endmodule

- What does CMOS stand for? VLSI? ASIC?
  This was in the series of quick questions in the interview at Analog Devices. We use these abbreviations daily, but not everyone remembers what they stand for.

- Design a COMBINATIONAL circuit that can divide the clock frequency by 2.

- Design a 2bit up/down counter with clear using gates. (No verilog or vhdl)

  we have a circular wheel with half painted black and the other half painted white. There are 2 censors mounted 45 degree apart at the surface of this wheel(not touching the wheel) which give a "1" for black and "0" for white passing under them. Design a circuit to detect which way the wheel is moving. Can not assume any fixed position for start.

  We have a fifo which clocks data in at 100mhz and clocks data out at 80mhz. On the input there is only 80 data in any order during each 100 clocks. In other words, a 100 input clock will carry only 80 data and the other twenty clocks carry no data (data is scattered in any order). How big the fifo needs to be to avoid data over/under-run.

- Instead of specifying SETUP and HOLD time, can we just specify a SETUP time for '1' and a SETUP time for '0'?

- Here some hardware digital design specific questions, offered by Suhas:
  (1) When will you use a latch and a flipflop in a sequential design?

(2) Design a 1-bit fulladder using a decoder and 2 "or" gates?

(3) You have a circuit operating at 20 MHz and 5 volt supply. What would you do to reduce the power consumption in the circuit- reduce the operating frequency of 20Mhz or reduce the power supply of 5Volts and why?

(4) In a nmos transistor, how does the current flows from drain to source in saturation region when the channel is pinched off?

(5) In a SRAM circuit, how do you design the precharge and how do you size it?

(6) In a PLL, what elements(like XOR gates or Flipflops) can be used to design the phase detector?

(7) While synthesis of a design using synopsys design compiler, why do you specify input and output delays?

(8) What difference do you see in the timing reports for a propogated clock and an ideal clock?

(9) What is timeborrowing related to Static timing anaylsis in Primetime?

In this article we are going to talk about CPU architecture.
RISC stands for reduced instruction set computer and CISC - for complex instruction set computer. The major difference is that RISC chips use simpler instructions sets to achieve higher clock frequencies and process more instructions per clock cycle than CISC processors. Typically CISC chips have a large amount of different and complex instructions. The philosophy behind it is that hardware is always faster than software, therefore one should make a powerful instructionset, which provides programmers with assembly instructions to do a lot with short programs. In common CISC chips are relatively slow (compared to RISC chips) per instruction, but use little (less than RISC) instructions. Intel and AMD, for example, develop CISC processors (x86) while Apple and SUN use RISC architecture. Major problem of RISC - they don't afford the widespread compatibility that x86 chips do.

logic questions

- How can you arrange for two people to stand on the same piece of newspaper and yet be unable to touch each other without stepping off the newspaper?

- How many 3-cent stamps are there in a dozen?

- A rope ladder hangs over the side of a ship. The rungs are one foot apart and the ladder is 12 feet long. The tide is rising at four inches an hour. How long will it take before the first four rungs of the ladder are underwater?

- Which would you rather have, a trunk full of nickels or a trunk half full of dimes?

- Steve has three piles of sand and Mike has four piles of sand. If they put them all together, how many do they have?

- In which sport are the shoes made entirely of metal?

- If the Vice-president of the United States should die, who would be President?

- How can you throw a golf ball with all your might and -- without hitting a wall or any other obstruction -- have the ball stop and come right back to you?

- When examining planets in our solar system, we usually find characteristics shared by multiple planets. Taking this into account, how many planets in our solar system have earthquakes?

- Find the English word that can be formed from all these letters: PNLLEEEESSSSS

Answers

Answers:

- Slide the newspaper half way under a closed door and ask the two people to stand on the bit of newspaper on their side of the door.

- There are twelve (not four).

- Actually, the ladder will rise with the ship!

- Dimes are smaller than nickels, so choose the dimes!

- If they put them all together, there will be one pile.

- Horse racing.

- The President.

- Throw the ball straight up.

- One. Only the earth has earthquakes.

- Sleeplessness.

Score:

10 right = You're a master of logic.

8 - 9 right = You're good... really good.

6 - 7 right = Not bad...

4 - 5 right = You need to practice.

2 - 3 right = You did terrible. But there is still hope that you "might" be able to improve with a lot of practice and hard work.

0 - 1 right = Uh oh... someone's pet is walking across the keyboard again... (we sincerely hope)